CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device comprising:

a CAM array;

a first counter circuit coupled to the CAM array, the first counter circuit being adapted to store an address value and to incrementally adjust the address value in response to a first control signal and to reset the address value to a start address in response to a second control signal;

a second counter circuit to store a limit value and to incrementally adjust the limit value in response to the second control signal; and

a compare circuit coupled to receive the address value from the first counter circuit and the limit value from the second counter circuit, the compare circuit being adapted to assert the second control signal if the address value and the limit value have a predetermined relationship.

2. The CAM device of claim 1 wherein the compare circuit is adapted to compare the address value to the limit value and to assert the second control signal if the address value and the limit value are equal.

3. The CAM device of claim 1 wherein the second counter is adapted to incrementally adjust the limit value in response to the second control signal after the second control signal has been delayed for a first delay time.

4. The CAM device of claim 1 wherein the first counter is adapted to incrementally adjust the

address value by increasing the address value by a predetermined amount.

5. The CAM device of claim 4 wherein the predetermined amount is one.

6. The CAM device of claim 1 wherein the first counter is adapted to incrementally adjust the address value by decreasing the address value by a predetermined amount.

7. The CAM device of claim 1 wherein the start address corresponds to a highest priority storage location in the CAM array.

8. The CAM device of claim 1 wherein the start address is a lowest address that corresponds to a storage location within the CAM array.

9. The CAM device of claim 1 wherein the start address is a highest address that corresponds to a storage location within the CAM array.

10. The CAM device of claim 1 further comprising a programmable storage element to store the start address.

11. The CAM device of claim 1 wherein the second counter circuit is responsive to a third signal to reset the limit value to an initial limit value.

12. The CAM device of claim 11 wherein the initial limit value is an address value that corresponds to a highest priority storage location within the CAM array.

13. The CAM device of claim 11 wherein the initial limit value is a lowest address that corresponds to a storage location within the CAM array.

14. The CAM device of claim 11 wherein the initial limit value is a highest address that corresponds to a storage location within the CAM array.

15. The CAM device of claim 11 further comprising a storage element to store the initial limit value.

16. The CAM device of claim 15 wherein the storage element is programmable to store the initial limit value during operation of the CAM device.

17. The CAM device of claim 1 wherein the second counter circuit is adapted to incrementally adjust the limit value by increasing the limit value by a predetermined amount.

18. The CAM device of claim 1 wherein the second counter is adapted to incrementally adjust the limit value by decreasing the limit value by a predetermined amount.

19. The CAM device of claim 1 further comprising a third counter circuit to store a block select value, the third counter being adapted to incrementally adjust the block select value in response to a third control signal and to assert the first control signal when the block select value reaches a predetermined value.

20. The CAM device of claim 1 wherein the first counter circuit is adapted to detect when the limit value has reached a predetermined limit value and, in response, to generate a third control signal, the CAM device further comprising a third counter circuit to store a block select value, the third counter circuit being adapted to incrementally adjust the block select value in response to the third control signal.

21. The CAM device of claim 20 wherein the third counter circuit is further adapted to reset the block select value to an initial block select value in response to a fourth control signal, and the CAM device further comprising:

a fourth counter circuit to store a block select limit and to incrementally adjust the block select limit in response to the fourth control signal; and

a block select compare circuit coupled to receive the block select value from the third counter circuit and the block select limit from the fourth counter circuit, the block select compare circuit being adapted to assert the fourth control signal if the block select value and the block select limit have a predetermined relationship.

22. The CAM device of claim 1 wherein:

the CAM array includes a plurality of rows of CAM cells and a plurality of word lines coupled respectively to the plurality of rows of CAM cells; and wherein the CAM device further comprises:

an address decoder coupled to the plurality of word lines and coupled to receive the address value from the first counter circuit, the address decoder being adapted to activate one of the plurality of word lines according to the address value such that a data word within the row of CAM cells coupled to the one of the plurality of word lines is output from the CAM array; and

an error detector coupled to receive the data word from the CAM array and having circuitry to determine whether the data word contains an error.

23. A method of operation within a content addressable memory (CAM) device, the method comprising:

accessing data stored at a first address value in a CAM array;

comparing the first address value with a second address value to determine if the first address value and the second address value have a predetermined relationship; and

incrementally adjusting the second address value if the first address value and the second address value have the predetermined relationship.

24. The method of claim 23 further comprising resetting the first address value to a start address if the first address value and the second address value have the predetermined relationship.

25. The method of claim 24 wherein resetting the first address value to a start address comprises resetting the first address value to a start address that corresponds to a highest priority storage location in the CAM array.

26. The method of claim 24 wherein resetting the first address value to a start address comprises resetting the first address value to a lowest address that corresponds to a storage location within the CAM array.

27. The method of claim 24 wherein resetting the first address value to a start address comprises resetting the first address value to a highest address that corresponds to a storage location within the CAM array.

28. The method of claim 23 further comprising incrementally adjusting the first address value if the first address value and the second address value do not have the predetermined relationship.

29. The method of claim 28 wherein incrementally adjusting the first address value comprises increasing the first address value by a predetermined amount.

30. The method of claim 28 wherein incrementally adjusting the first address value comprises decreasing the first address value by a predetermined amount.

31. The method of claim 23 wherein comparing the first address value with the second address value to determine if the first address value and the second address value have a predetermined relationship comprises determining if the first address value and the second address value are equal.

32. The method of claim 23 wherein comparing the first address value with the second address value to determine if the first address value and second address value have a predetermined relationship comprises determining if the first address value is greater than the second address value.

33. The method of claim 23 wherein incrementally adjusting the second address value comprises increasing the second address value by a predetermined amount.

34. The method of claim 23 wherein incrementally adjusting the second address value comprises decreasing the second address value by a predetermined amount.

35. The method of claim 23 further comprising:

receiving a reset signal; and

resetting the second address value to an initial value.

36. The method of claim 35 wherein resetting the second address value to an initial value comprises resetting the second address value to an initial value that corresponds to a highest priority storage location in the CAM array.

37. The method of claim 35 wherein resetting the second address value to an initial value comprises resetting the second address value to a lowest address that corresponds to a storage location within the CAM array.

38. The method of claim 35 wherein resetting the second address value to an initial value comprises resetting the second address value to a highest address that corresponds to a storage location within the CAM array.

39. A content addressable memory (CAM) device comprising:

means for accessing data stored at a first address value in a CAM array;

means for comparing the first address value with a second address value to determine if the first address value and the second address value have a predetermined relationship; and

means for incrementally adjusting the second address value if the first address value and the second address value have the predetermined relationship.

40. The CAM device of claim 39 further comprising means for resetting the first address value to a start address if the first address value and the second address value have the predetermined relationship.

41. The CAM device of claim 39 further comprising means for incrementally adjusting the first

address value if the first address value and the second address value do not have the predetermined relationship.

42. The CAM device of claim 41 wherein the means for incrementally adjusting the first address value comprises means for increasing the first address value by a predetermined amount.

43. The CAM device of claim 41 wherein the means for incrementally adjusting the first address value comprises means for decreasing the first address value by a predetermined amount.

44. A content addressable memory (CAM) device comprising:

a CAM array having a plurality of rows of CAM cells;

a first counter to store an address for one of the rows of CAM cells;

a second counter circuit to store a limit value;

a compare circuit coupled to the first and second counters to compare the address with the limit value; and

an address decoder coupled to the first counter and the CAM array to select one of the rows of CAM cells corresponding to the address.

45. The CAM device of claim 44 further comprising an error detector coupled to the CAM array to receive a data word from the selected one the rows of CAM cells and to detect whether there is an error in the data word.

46. The CAM device of claim 44 wherein the CAM array comprises a plurality of CAM array blocks, and wherein the CAM device further comprises a third counter coupled to the first

counter, the third counter to store a block select value to select one of the CAM array blocks.

47. The CAM device of claim 46 wherein the third counter is coupled to receive the address from the first counter.

48. The CAM device of claim 46 wherein the first counter is coupled to receive the block select value from the third counter.

49. The CAM device of claim 1 further comprising:

a fourth counter to store a block select limit; and

a second compare circuit coupled to the third and fourth counters to compare the block select value and the block select limit.

50. A content addressable memory (CAM) device comprising:

a CAM array having a plurality of rows of CAM cells; and

address circuitry coupled to the plurality of rows of CAM cells and adapted to access the rows in a biased sequence order.

51. The CAM device of claim 50 further comprising an error detector coupled to the CAM array to receive data from the accessed rows and detect whether there is an error in the data.

52. The CAM device of claim 50 wherein the address circuitry comprises:

a first counter;

a second counter;

a compare circuit coupled to outputs of the first and second counters; and

an address decoder coupled to the first counter and the rows of CAM cells.

53. The CAM device of claim 50 wherein the CAM array includes a plurality of CAM array blocks each including a plurality of rows of CAM cells that is a subset of the plurality of rows of CAM cells in the CAM array, and wherein the address circuitry is adapted to access the rows included within each of the CAM array blocks in a biased sequence order.

54. The CAM device of claim 53 wherein the address circuitry is further adapted to access the blocks in a linear sequence order.

55. The CAM device of claim 53 wherein the address circuitry is further adapted to access the blocks in a biased sequence order.

56. The CAM device of claim 53 wherein the address circuitry comprises:

a first counter;

a second counter;

a first compare circuit coupled to outputs of the first and second counters;

an address decoder coupled to the first counter and the rows of the CAM array blocks; and

a third counter coupled to the first counter.

57. The CAM device of claim 56 further comprises:

a fourth counter; and

a second compare circuit coupled to outputs of the third and fourth counters.

58. A method of operation within a content addressable memory (CAM) device, the method

comprising:

accessing rows of CAM cells in a CAM array in a biased sequence order; and

detecting whether data stored in each accessed row contains an error.

59. The method of claim 58 wherein the CAM array includes a plurality of CAM array blocks, and the method further comprises accessing rows of CAM cells in a first one of the CAM array blocks in a biased sequence order.

60. The method of claim 59 further comprising selecting the CAM array blocks in a linear sequence order.

61. The method of claim 59 further comprising selecting the CAM array blocks in a biased sequence order.